micromachines

Article

Effect of Metal Oxide Semiconductor Field-Effect Transistor Output Parasitic Capacitance on Efficiency in Full-Bridge LLC DC/DC Converters

Ming-Hung Chen * and Chia-Wen Hsieh

Department of Electrical Engineering, Ming Chi University of Technology, New Taipei City 243303, Taiwan; m08128014@mail2.mcut.edu.tw

* Correspondence: mhchen@mail.mcut.edu.tw; Tel.: +886-2-29089899 (ext. 5211)

Abstract: This study analyzed the efficiency impact of a MOSFET output parasitic capacitance (C_{oss}) on a full-bridge LLC DC/DC converter. The core of the converter was the control chip for a half-bridge LLC DC/DC converter, and the output signal of the chip controlled the first-arm power transistors of the primary side of the converter. The coupling transformer reversed the output signal to control the primary side of the second arm of the power transistor. The full-bridge converter comprises a half-bridge control chip that converts the high-voltage DC power supply to a low-voltage DC power supply, which is then synchronously rectified and supplied to the load. The primary side of the power transistor achieves a zero-voltage switching (ZVS) state through the resonance of the LLC converter. This design gives the converter high power density and a simple structure. Furthermore, to determine the appropriate output parasitic capacitance for improving converter efficiency, this study analyzed the effect of the output parasitic capacitance on the switching loss and conduction loss of the power transistor on the basis of the output parasitic capacitance of the primary-side power transistor. A 1200 W converter prototype was fabricated in this study, and when the output was 300 W, efficiency increased from 92.603% to 93.462%, a 0.859% increase. The empirical results verified the feasibility of the proposed theory.

Keywords: output parasitic capacitance (C_{oss}); full-bridge LLC DC/DC converter; zero voltage switching (ZVS) state

Citation: Chen, M.-H.; Hsieh, C.-W. Effect of Metal Oxide Semiconductor Field-Effect Transistor Output Parasitic Capacitance on Efficiency in Full-Bridge LLC DC/DC Converters. *Micromachines* **2024**, *15*, 309. https://doi.org/10.3390/mi15030309

Academic Editors: Chun-An Cheng, En-Chih Chang, Chien-Hsuan Chang and Ching-Min Lee

Received: 25 January 2024
Revised: 14 February 2024
Accepted: 20 February 2024
Published: 23 February 2024

1. Introduction

Electric vehicles, cloud technology, and artificial intelligence are emerging industries whose development is hindered by power requirements. In particular, electric vehicles are more efficient at converting power from their power plant to vehicular motion relative to conventional combustion-engine vehicles—where the conversion efficiency of an electric vehicle is determined both by the motor and the overall power conversion system. In addition, cloud technology will become increasingly important as remote work becomes the norm. Powerful servers and high-power systems are required to handle large volumes of data being transmitted in and out of the cloud. These developments necessitate the design of a compact, high-conversion-efficiency, and high-power system [1].

DC/DC converters are either isolated or non-isolated depending on whether the converter has a transformer. Common non-isolated converters include the buck converter, boost converter, and buck-boost converter. These converters have simpler topologies and thus simpler circuitry; however, they cannot achieve high conversion efficiency when the step-down ratio is high due to the lack of a transformer and also cannot provide electrical isolation. Non-isolated DC/DC converters are more commonly found in buck-boost applications at the back end of isolated converters.

Common isolated converters include the flyback converter, half-bridge converter, and full-bridge converter. Isolated converters have transformers and therefore feature

high step-down ratios and electrical isolation capability [2–7]. Flyback converters have simple structures and can be constructed with a few components; because these converters have only one power transistor, the voltage stress is rather high, and flyback converters are thus typically low-power converters. Half-bridge converters have one more power transistor than flyback converters and consequently lower voltage stress. Because the transformer inputs are half-wave signals, the operating current of the power transistor is higher than that of flyback converters. In applications with high input voltages and high power, choosing an appropriate power transistor is critical. Relative to half-bridge converters, full-bridge converters have two more power transistors, which reduce voltage stress, and use full-wave signals as transistor inputs, which further reduce the operating current of the power transistors while increasing control complexity. These converters are primarily used in high-voltage and high-power applications [8–10].

The LLC resonant converter selected in this study can be employed in both half-bridge and full-bridge architectures and uses pulse frequency modulation to maintain the duty cycle of the transistor at approximately 50% by modulating the driving signal to modulate the power output. The LLC resonant converter also has the following features [11–13]:

- In any state, the primary-side power transistor of the converter remains in the ZVS state; in a fully loaded state, the secondary-side rectifier enters the zero current switching state;
- When fully loaded, the switching frequency of the converter will be equal to the resonant frequency, improving its performance;
- The cutoff switching current of the power transistor can be lowered by increasing L_m, thus reducing switching loss;
- L_r and L_m can be integrated or isolated. Integrating the two can effectively reduce the size of the converter and save on costs, whereas isolating the two enables the precise control of the resonant inductance value and enhances converter efficiency.

Table 1 presents the basic characteristics of an LLC resonant transformer when used in a half-bridge converter or a full-bridge converter.

Table 1. Half-bridge LLC resonant converter versus full-bridge LLC resonant converter.

Converter	Half-Bridge LLC Resonant Converter	Full-Bridge LLC Resonant Converter
Power transistors	2	4
Resonance slot reference point	$+V_{in}$ and 0	$+V_{in}$ and $-V_{in}$
Control complexity	Simple	Complex
Applied power	Low power	High power
Control chips	Common	Does not exist

The full-bridge architecture is generally used in high-power and high-efficiency converters. However, given the lack of commercially available control chips for full-bridge LLC converters, in this paper, a full-bridge LLC resonant converter was fabricated using a half-bridge LLC resonant control chip. In order to maintain full-bridge power transistors in the ZVS states with a half-bridge LLC resonant control chip, the output parasitic capacitance of the first-arm power transistors was determined so that they can be added appropriately to improve the converter efficiency.

2. Operating Principles

Figure 1 illustrates the circuitry of the full-bridge LLC resonant converter featured in this study. The parameters labeled in the diagram are presented in Table 2. If the transformer in the converter were ideal, the primary side and secondary side would each form independent loops. The primary side is controlled by using the half-bridge LLC resonant control chip to drive the first-arm power transistors (Q_1 and Q_2), then reversing

the first-arm signal through the coupling transformer to drive the second-arm power transistors (Q_3 and Q_4). The secondary side comprises a full-wave rectification circuit, which is equivalent to a diode (D_{r1} and D_{r2}) in circuit analysis.

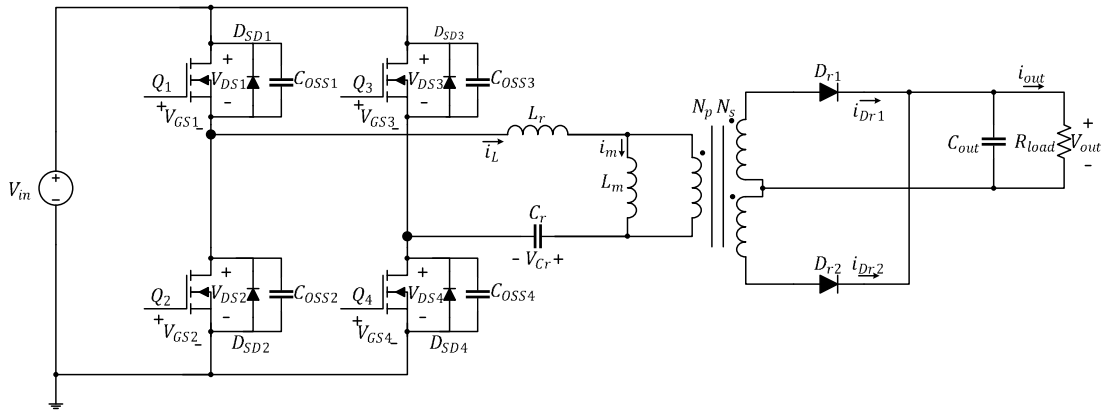

Figure 1. Circuitry of the full-bridge LLC resonant converter.

Table 2. Circuit symbols.

Symbols	Names	Symbols	Names
N_p	Number of turns in the primary side	N_s	Number of turns in the secondary side
Q_1	First-arm high-side power transistor	Q_2	First-arm low-side power transistor
Q_3	Second-arm high-side power transistor	Q_4	Second-arm low-side power transistor
C_{oss1}	Q_1 output parasitic capacitor	C_{oss2}	Q_2 output parasitic capacitor
C_{oss3}	Q_3 output parasitic capacitor	C_{oss4}	Q_4 output parasitic capacitor
$D_{SD(1\sim4)}$	Body diode of the power transistor	C_r	Resonant capacitor
L_r	Resonant inductor	L_m	Magnetizing inductor
D_{r1}	Positive half-cycle rectifier diode on the secondary side	D_{r2}	Negative half-cycle rectifier diode on the secondary side
C_{out}	Output filter capacitor	R_{load}	Secondary-side load resistor
V_{in}	Input voltage	$V_{GS(1\sim4)}$	Power transistor gate-source voltage
V_{Cr}	Resonant capacitor voltage	$V_{DS(1\sim4)}$	Power transistor drain-source voltage
V_{out}	Output voltage	i_{out}	Output current
i_L	Resonant inductor current	i_m	Magnetizing inductor current
i_{Dr1}	D_{r1} forward current	i_{Dr2}	D_{r2} forward current

LLC resonant converters typically operate either in the inductive region or the resistive region, which are differentiated by the current mode of the converter. Figure 2 is a waveform diagram of the LLC resonant converter operating in the resistive region [14].

In Figure 2, the circuitry of the full-bridge LLC resonant converter has six modes, designated t_0 to t_6; the circuit operations are as follows [15–17]:

- Mode 1: ($t_0 \leq t < t_1$)

The current path in this mode is depicted in Figure 3. At time t_0, Q_1 and Q_4 are turned on while Q_2 and Q_3 are cut off; in addition, i_L flows through Q_1 and Q_4 and increases positively in a sinusoidal manner while i_m increases linearly. At this time, because $i_L > i_m$, the primary side of the converter has a positive half-cycle voltage, and the energy is transmitted to the secondary side through the transformer. D_{r1} is turned on and generates i_{Dr1} to provide energy to C_{out} and R_{load}. In this mode, L_m is clamped by the output voltage to nV_o and is not involved in the resonance; only L_r and C_r are involved.

- Mode 2: ($t_1 \leq t < t_2$)

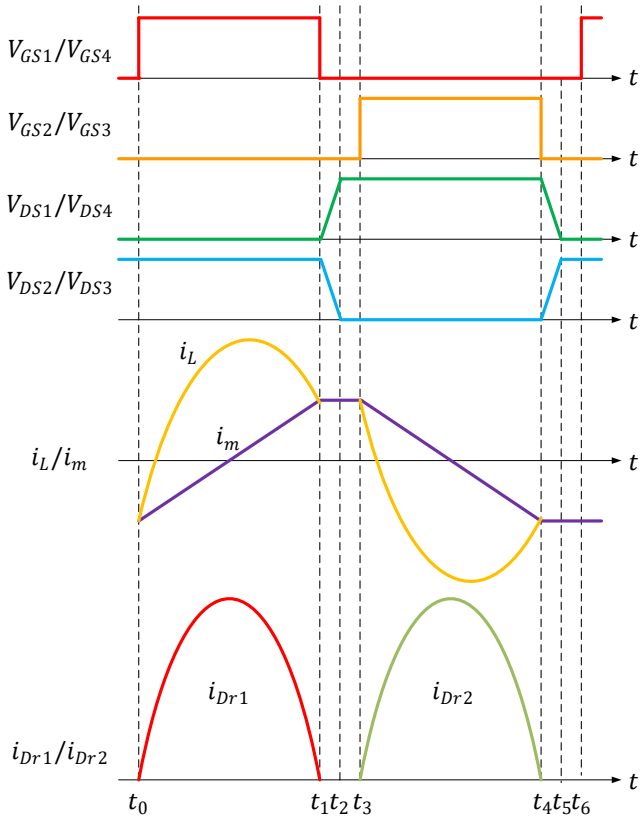

Figure 2. Waveform of a full-bridge LLC resonant converter in operation.

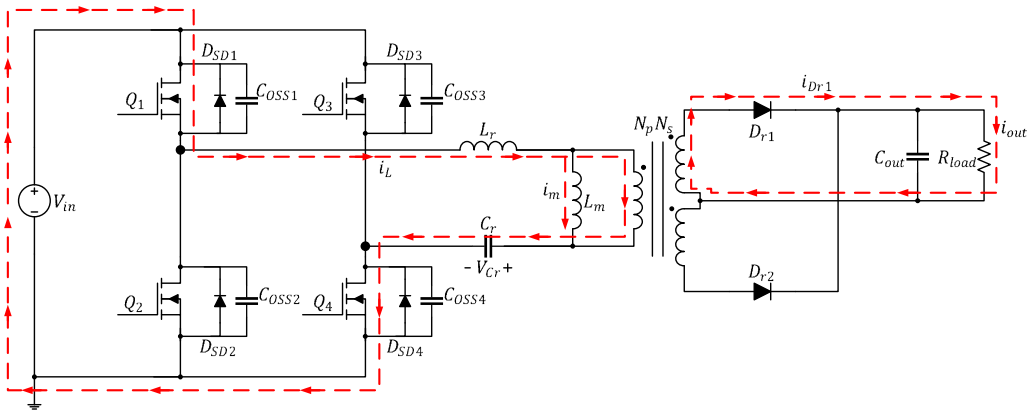

Figure 3. Current path of the full-bridge LLC resonant converter in Mode 1 ($t_0 \leq t < t_1$).

The current path in this mode is depicted in Figure 4. During this interval, all four power transistors are cut off; because the inductor current cannot be cut off immediately, i_L and i_m remain equal, and their directions do not change. The converter makes use of this time interval to transfer energy from the output parasitic capacitor, charging C_{oss1} and C_{oss4} and discharging C_{oss2} and C_{oss3}. During this time, the transformer is not transferring energy, and, consequently, i_{Dr1} on the secondary side drops to zero; R_{load} is supplied power by C_{out}. L_m is no longer clamped by the output voltage and becomes part of the resonance alongside L_r and C_r; at this time, i_L can be regarded as a fixed current coming from the source.

- Mode 3: ($t_2 \leq t < t_3$)

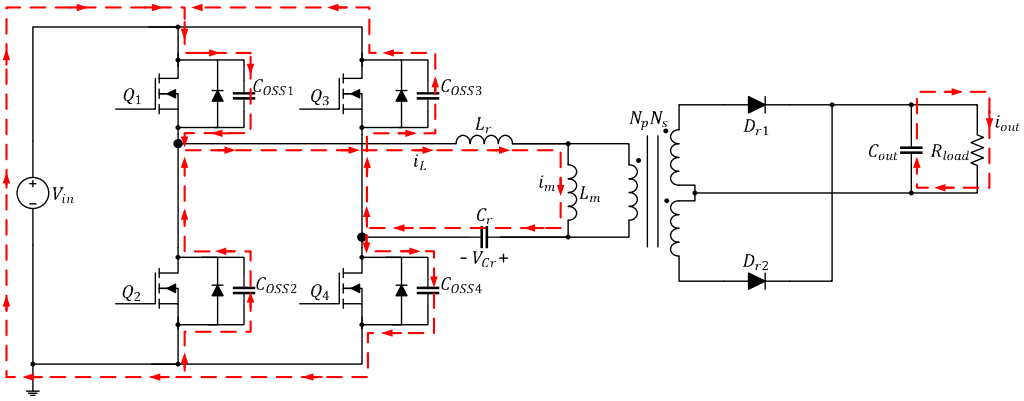

Figure 4. Current path of the full-bridge LLC resonant converter in Mode 2 ($t_1 \leq t < t_2$).

The current path in this mode is depicted in Figure 5. During this interval, the four power transistors remain cut off. Again, because the inductor current cannot be cut off immediately, i_L and i_m remain equal, and their directions do not change. Furthermore, the charging and discharging output parasitic capacitors on the power transistor have been completed, and the remaining energy now flows through the body diode rather than the output parasitic capacitors as before; consequently, the current from the converter flows through D_{SD2} and D_{SD3} during this interval, and the transformer continues to have no energy to transfer. R_{load} is still supplied power by C_{out}.

- Mode 4: ($t_3 \leq t < t_4$)

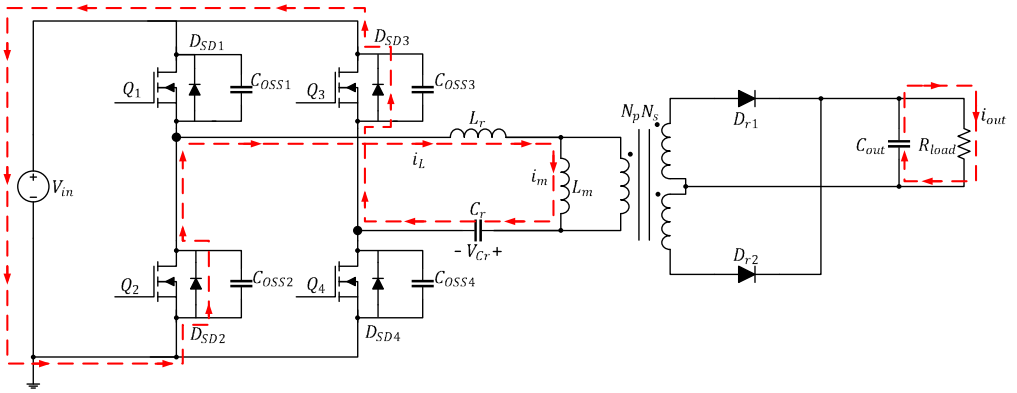

Figure 5. Current path of the full-bridge LLC resonant converter in Mode 3 ($t_2 \leq t < t_3$).

The current path in this mode is depicted in Figure 6. At time t_3, Q_2 and Q_3 are turned on, and Q_1 and Q_4 are cut off; i_L passes through Q_2 and Q_3 and increases negatively in a sinusoidal manner, whereas i_m decreases linearly. At this time, because $i_L < i_m$, the primary side of the converter has a negative half-cycle voltage, and the energy is transmitted to the secondary side through the transformer. D_{r2} is turned on and generates i_{Dr2} to provide energy to C_{out} and R_{load}. In this mode, L_m is clamped by the output voltage to nV_o and is not involved in the resonance; only L_r and C_r are involved.

- Mode 5: ($t_4 \leq t < t_5$)

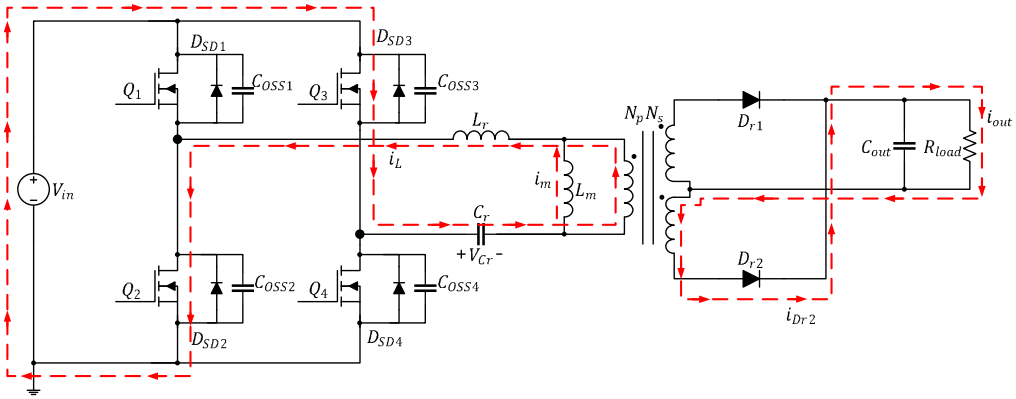

Figure 6. Current path of the full-bridge LLC resonant converter in Mode 4 ($t_3 \leq t < t_4$).

The current path in this mode is depicted in Figure 7. During this interval, the four power transistors are cut off; because the inductor current cannot be cut off immediately, i_L and i_m remain equal, and their directions do not change. Furthermore, the output parasitic capacitors of Q_2 and Q_3 are charged, and the output parasitic capacitors of Q_1 and Q_4 are discharged. During this time, the transformer is not transferring energy; consequently, i_{Dr2} on the secondary side drops to zero, and R_{load} is supplied power by C_{out}. L_m is no longer clamped by the output voltage and becomes part of the resonance alongside L_r and C_r; at this time, i_L can be regarded as fixed current from the source.

- Mode 6: ($t_5 \leq t < t_6$)

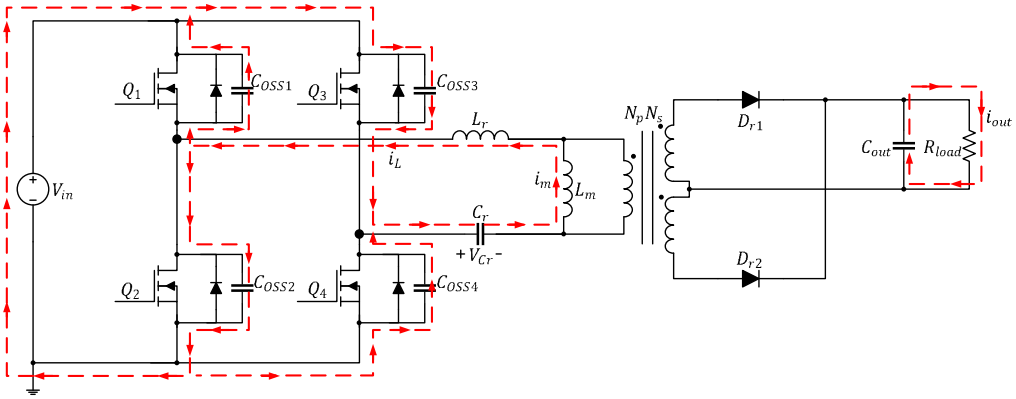

Figure 7. Current path of the full-bridge LLC resonant converter in Mode 5 ($t_4 \leq t < t_5$).

The current path in this mode is depicted in Figure 8. During this interval, the four power transistors remain cut off. Again, because the inductor current cannot be cut off immediately, i_L and i_m remain equal, and their directions do not change. Furthermore, the charging and discharging output parasitic capacitors on the power transistor have been completed, and the remaining energy now flows through the body diode rather than the output parasitic capacitors as before; consequently, the current from the converter flows through D_{SD1} and D_{SD4} during this interval, and the transformer continues to have no energy to transfer. R_{load} is still supplied power by C_{out}. At this point, the switching cycle is completed and starts again.

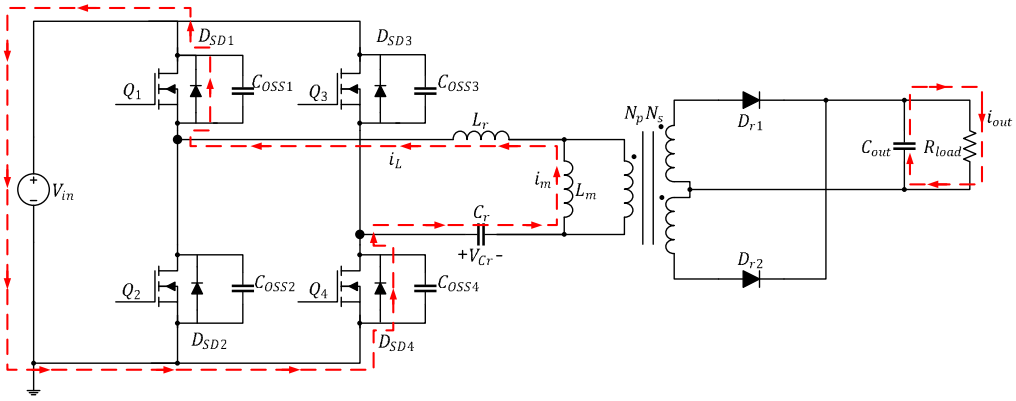

Figure 8. Current path of the full-bridge LLC resonant converter in Mode 5 ($t_5 \leq t < t_6$).

3. Effect of Output Parasitic Capacitor on Converter Efficiency

When the LLC resonant converter is under a full load range, the primary-side power transistor operates in the ZVS state. The converter resonates during the dead time to transfer the energy from C_{OSS} of the power transistor (Figure 6). If the dead time is too short, the C_{OSS} energy cannot be fully transferred, resulting in switching loss. In addition, energy has time to flow through the body diode of the power transistor if the dead time is overly long, increasing the conduction loss of the diode. Hence, the overall efficiency of the converter is affected by the amount of dead time. In practice, the dead time only lasts up until the conversion of C_{OSS} energy is complete. Therefore, the half-bridge LLC resonant control chip employed in this paper adjusts the length of the dead time by detecting whether the C_{OSS} energy has been released. The time needed to release the C_{OSS} energy is determined by the current load, which means that each load has a corresponding C_{OSS} energy release time, which is the corresponding dead time.

The amount of dead time affects the switching loss and conduction loss of a power transistor. When the system is under a heavy load, the power loss of the converter comes primarily from the iron loss and copper loss of the transformer, resulting in milder effects from switching loss and conduction loss of the power transistor. The effects of dead time under a light load were analyzed in this study. Light loads function in the inductive region, where the operating state is different from that in the resistive region—when the converter is in the resistive region, its current is in critical conduction mode, and, consequently, the transformer has no energy to transfer during the dead time. When the converter is in the inductive region, the current is in a continuous conduction mode, and the transformer continues to transfer energy during the dead time, as depicted in Figure 9; the equivalent circuit is shown in Figure 10.

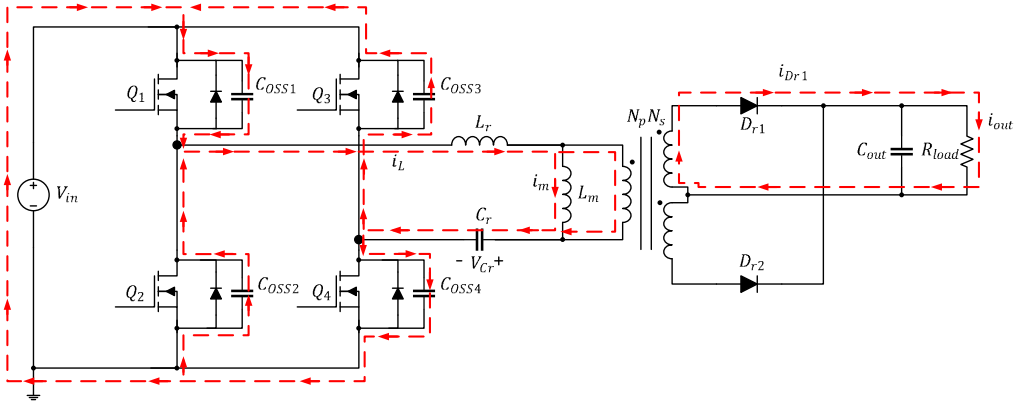

Figure 9. Full-bridge LLC resonant converter under a light load, Mode 2.

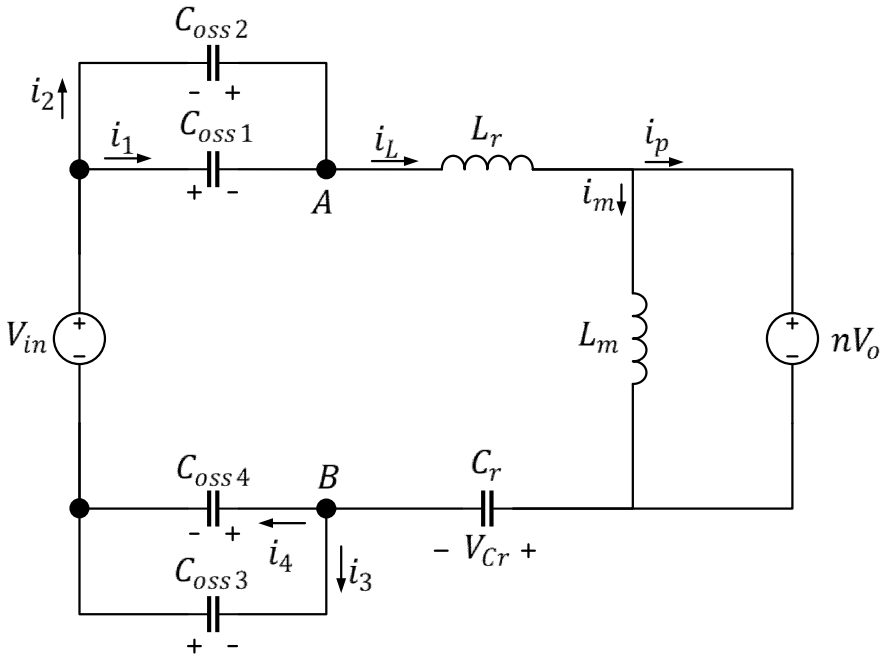

Figure 10. Equivalent circuit of the full-bridge LLC resonant converter under a light load, Mode 2.

Based on the direction of current, the converter stores energy in C_{oss1} and C_{oss4} and discharges energy from C_{oss2} and C_{oss3}; if the energy transferred in the loop is fixed, the following can be obtained:

$$Q_{AB} = C_{oss} V_{AB} = i_L t_{ZVS} \tag{1}$$

Here, V_{AB} and Q_{AB} are the resonant tank voltage and total charge, and C_{oss} is a pair of output parasitic capacitors (either C_{oss1} and C_{oss4} or C_{oss2} and C_{oss3}); t_{ZVS} is the dead time needed to reach ZVS. If the energy being transferred is fixed, in each state, only one pair of output parasitic capacitors is fully charged. According to Figure 9, transferring the loop energy to C_{oss1} and C_{oss4} at this time results in the following:

$$(C_{oss1} // C_{oss4}) V_{AB} = i_L t_{ZVS} \tag{2}$$

If the input voltage of the resonant tank is $+V_{in}$, then, according to Figure 10,

$$(C_{oss1} // C_{oss4}) V_{in} = i_L t_{ZVS} \tag{3}$$

$$i_L = i_m + i_p \tag{4}$$

$$i_L = \frac{nV_{out}}{L_m} t_{ZVS^2} + \frac{I_{out}}{n} t_{ZVS} \tag{5}$$

In Equations (3) and (5), the time needed to reach ZVS in ideal conditions is as follows:

$$(C_{oss1} // C_{oss4}) V_{in} = \frac{nV_{out}}{L_m} t_{ZVS^2} + \frac{I_{out}}{n} t_{ZVS} \tag{6}$$

$$\frac{nV_{out}}{L_m} t_{ZVS^2} + \frac{I_{out}}{n} t_{ZVS} - (C_{oss1} // C_{oss4}) V_{in} = 0 \tag{7}$$

$$t_{ZVS} = \frac{-\frac{I_{out}}{n} \pm \sqrt{\left(\frac{I_{out}}{n}\right)^2 + 4\left(\frac{nV_{out}}{L_m}\right)(C_{oss1} // C_{oss4}) V_{in}}}{2\frac{nV_{out}}{L_m}} \tag{8}$$

A greater I_o value corresponds to a heavier load and a shorter time required to reach ZVS. Therefore, when I_o = 0 A, the longest ZVS time of the converter is t_{ZVS} = 115.576 ns.

In this study, the efficiency of the converter under light loads was adjusted, and when the load was 300 W, ideally, $t_{ZVS} = 26.641$ ns.

The primary-side power transistors of the LLC resonant converter can enter the ZVS state under any load. The first-arm power transistors are driven by a half-bridge LLC resonant controller chip, and the second-arm power transistors are driven by the coupling transformer loop; as such, the controller chip is unable to detect the state of the second-arm power transistors. Furthermore, the coupling transformer loop causes signal delays, leading to errors in the driving times of the first-arm and second-arm power transistors; consequently, the second arm is unable to enter the ZVS state.

All four power transistors can enter the ZVS state by adjusting the first-arm C_{oss} and extending the converter dead time. If any pair of output parasitic capacitors have the same amount of energy, then

$$Q_{Coss1} = Q_{Coss4} \tag{9}$$

$$\frac{i_1}{V_{Coss1}} t_{ZVS1} = \frac{i_4}{V_{Coss4}} t_{ZVS2} \tag{10}$$

Here, V_{Coss1} and V_{Coss4} are the voltages of the Q_1 and Q_4 output parasitic capacitors, respectively, and t_{ZVS1} and t_{ZVS2} are the dead times needed by the first and second arms, respectively. According to Kirchhoff's circuit laws, the sum of the potential differences across all components in the loop is zero. Therefore, in the loop, $V_{Coss} = V_{in}$, yielding

$$\frac{i_L}{V_{in}} t_{ZVS1} = \frac{i_L}{V_{in}} t_{ZVS2} \tag{11}$$

Due to the time differences between the first-arm and second-arm transistors, the second-arm power transistors were unable to discharge all of their energy during the dead time, indicating a need for more time. Hence, $t_{ZVS1} < t_{ZVS2}$, and by entering t_{ZVS2} into Equation (6), we obtain:

$$\frac{nV_o}{L_m} t_{ZVS2^2} + \frac{I_o}{n} t_{ZVS2} - (C_{oss,New}) V_{in} = 0 \tag{12}$$

$$C_{oss,New} = \frac{\frac{nV_o}{L_m} t_{ZVS2^2} + \frac{I_o}{n} t_{ZVS2}}{V_{in}} \tag{13}$$

$$C_{oss1} + C_{ossX} = C_{oss,New} \tag{14}$$

where $C_{oss,New}$ is the adjusted output parasitic capacitance of the first-arm power transistors.

Using Equation (13), we find the appropriate first-arm C_{oss} is 90.49 pF, and, using Equation (14), we determine that the first-arm power transistors must be connected in parallel with an output capacitor of 40.49 pF.

After the four primary-side power transistors have entered the ZVS state, if the first-arm C_{oss} continues to be increased to extend the converter dead time, because the first-arm power transistors are monitored by the controller chip, the first arm remains in the ZVS state; however, the second-arm power transistors are not monitored, and, therefore, after the energy transfer is complete, the remaining energy of the second-arm C_{oss} flows through the body diode of the power transistors, as illustrated in Figure 11; see Figure 12 for the equivalent circuit.

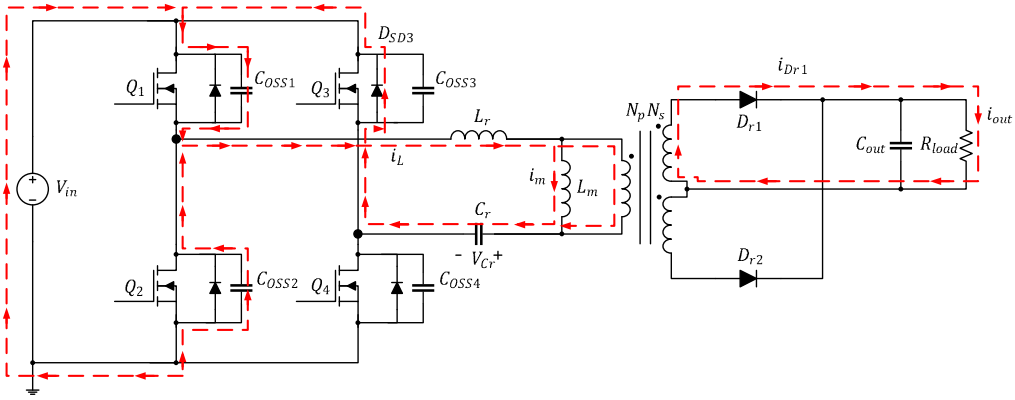

Figure 11. Full-bridge LLC resonant converter under light load and extended dead time in Mode 2.

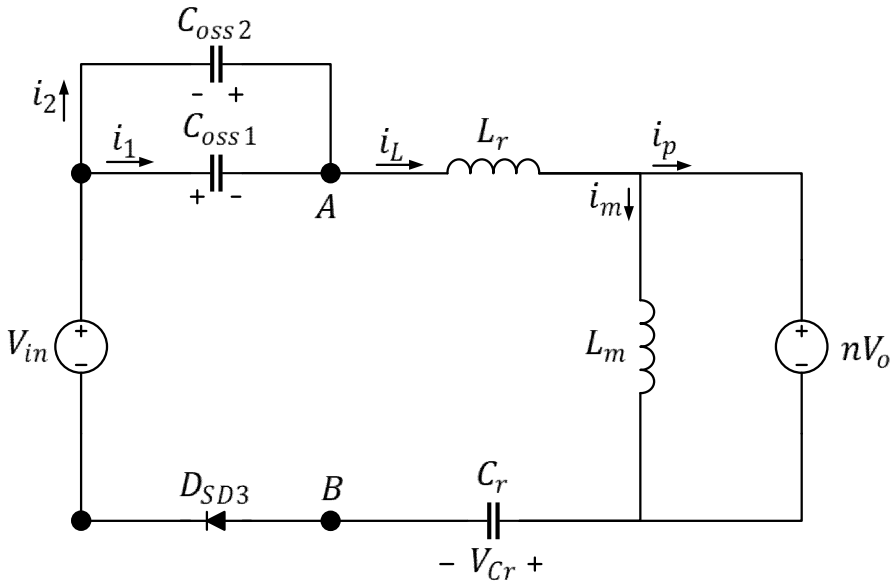

Figure 12. Equivalent circuit of the full-bridge LLC resonant converter under light load and extended dead time in Mode 2.

As illustrated in Figure 12, an excessive C_{oss} results in overly long dead times; the conduction loss increased by the second-arm power transistors is

$$P_{ZVS,Con} = f_r i_L V_{D_{SD3}} (t_{ZVS,exc} - t_{ZVS,mod}) \quad (15)$$

where

$t_{ZVS,exc}$: excessive time in the ZVS state
$t_{ZVS,mod}$: optimal time in the ZVS state

Equation (14) indicates that when the dead time exceeds $t_{ZVS,mod}$, for each additional 10 ns, the conduction loss by the body diode increases by 8.2 μW.

The relationships between C_{oss} and the switching loss and conduction loss of the primary-side power transistors of the full-bridge LLC resonant converter can be derived from the aforementioned equations (Figure 13).

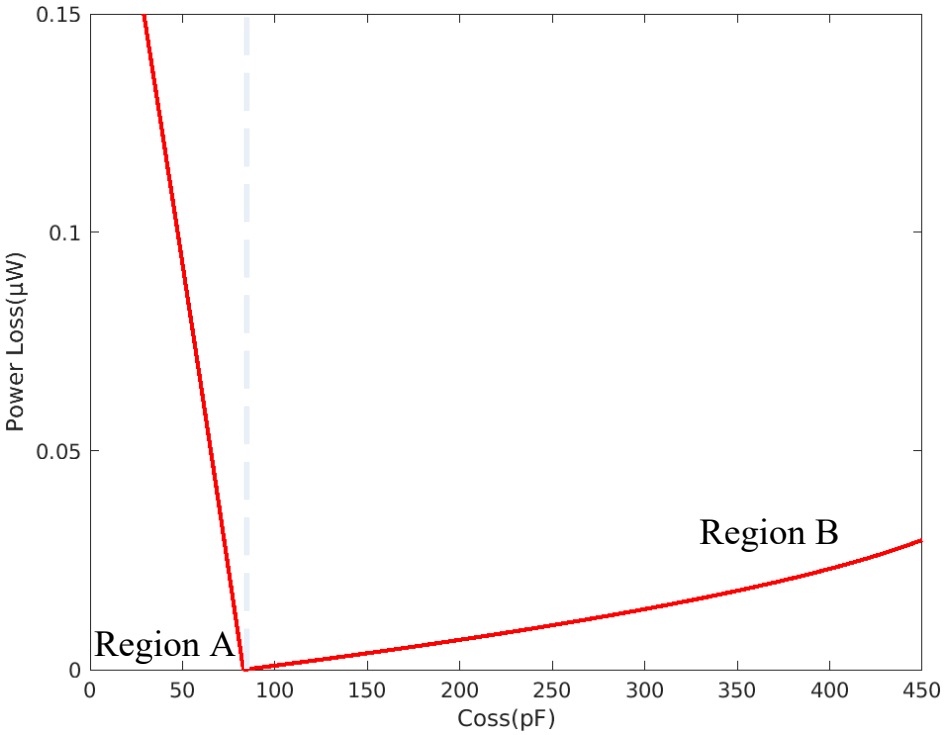

Figure 13. Effect of C_{oss} on switching loss and conduction loss of the power transistors.

The left (Region A) and right (Region B) partitions of the curve in Figure 13 correspond to values lower and higher than the suitable C_{oss} value, respectively. Region A is the switching loss caused by the inability of the second-arm power transistors to fully transfer the C_{oss} energy during the dead time, which is too short because C_{oss} is too low. Region B is the conduction loss caused by the induction current continuing to flow though the body diode after the second-arm power transistors have finished transferring C_{oss} because the dead time is too long. The figure demonstrates that loss increases when C_{oss} is too high or too low. Furthermore, the loss in Region A is greater than the loss in Region B, and therefore, switching loss must be minimized in the design.

4. Experimental Results

The circuitry of the full-bridge LLC resonant converter combined with secondary-side synchronous rectification is depicted in Figure 14; the component specifications are presented in Table 3.

The converter's poor efficiency under light loads was improved by adjusting the C_{oss} of the power transistors. According to the calculation results of Equation (8), the first-arm power transistors on the primary side must be connected in parallel to a 40.94 pF capacitor to achieve the appropriate dead time; because the C_{oss} cross voltage of each power transistor is V_{in}, a capacitor with a capacitance of 10pF/1kV was selected in this study. As indicated in Figure 15, overlap between the power transistors was greatly reduced, indicating noticeable ZVS states, and the measured temperatures of the two low-side power transistors was also greatly reduced. Prior to the adjustments, the second arm was 10 °C warmer than the first arm; after the adjustments, the temperature difference dropped to 0.5 °C.

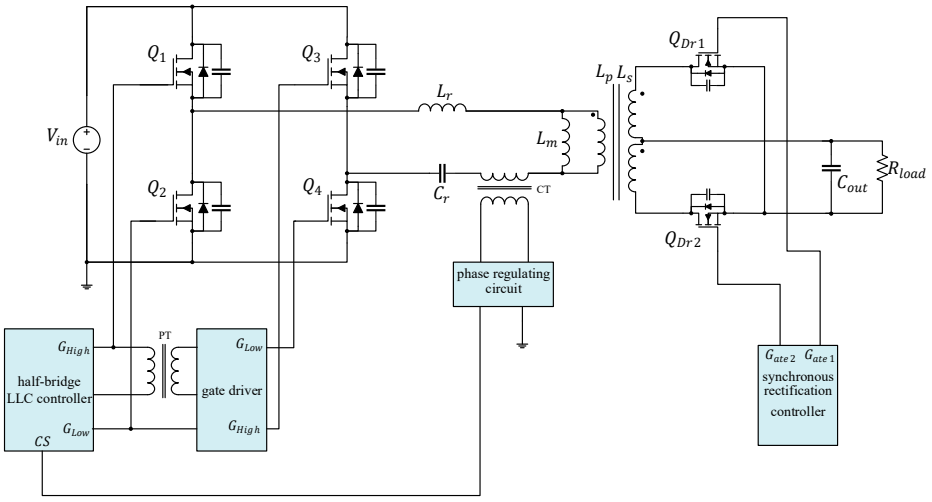

Figure 14. Complete schema of the full-bridge LLC resonant converter.

Table 3. Converter specifications.

Specifications	Values
Input voltage range (V_{in} Range)	350 V_{dc} ~ 420 V_{dc}
Output voltage (V_{out})	48 V_{dc}
Resonant frequency (f_r)	82 kHz
Resonant capacitance (C_r)	66 nF
Resonant induction (L_r)	60 µH
Magnetizing inductance (L_m)	520 µH
Primary-side LLC resonant controller chip	NCP13992
Secondary-side synchronous rectification controller chip	NCP4318

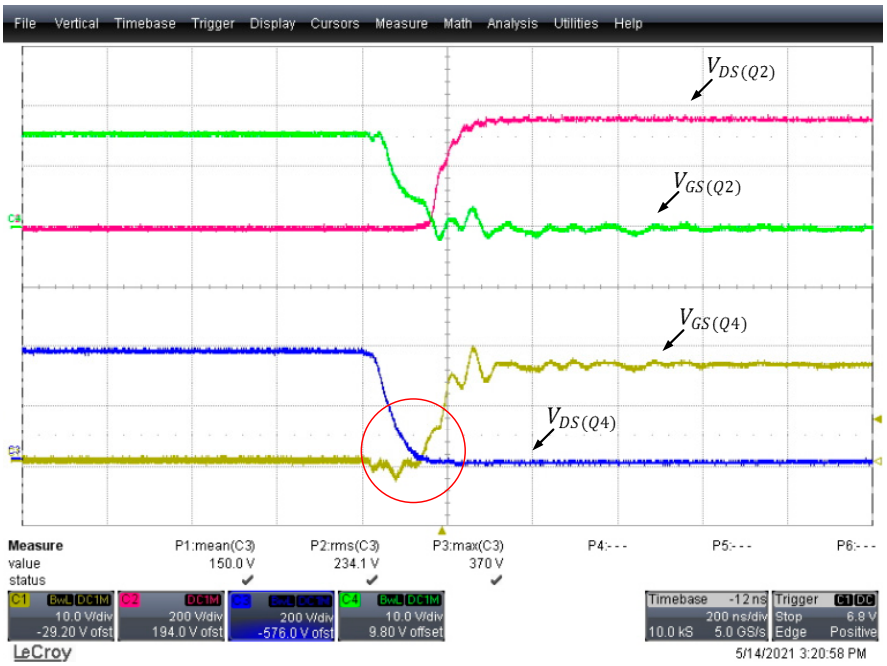

Figure 15. Dead time after adjusting the first-arm C_{oss} of the full-bridge LLC resonant converter.

According to the results of Equation (15), if the first-arm C_{oss} is continually increased, the first arm remains in the ZVS state, while in the second arm, the remaining energy flowing through the body diode of the power transistors during the unnecessary dead time leads to conduction loss. As shown in Figure 16, after the transfer of the parasitic output capacitor energy, the power transistors failed to immediately change states.

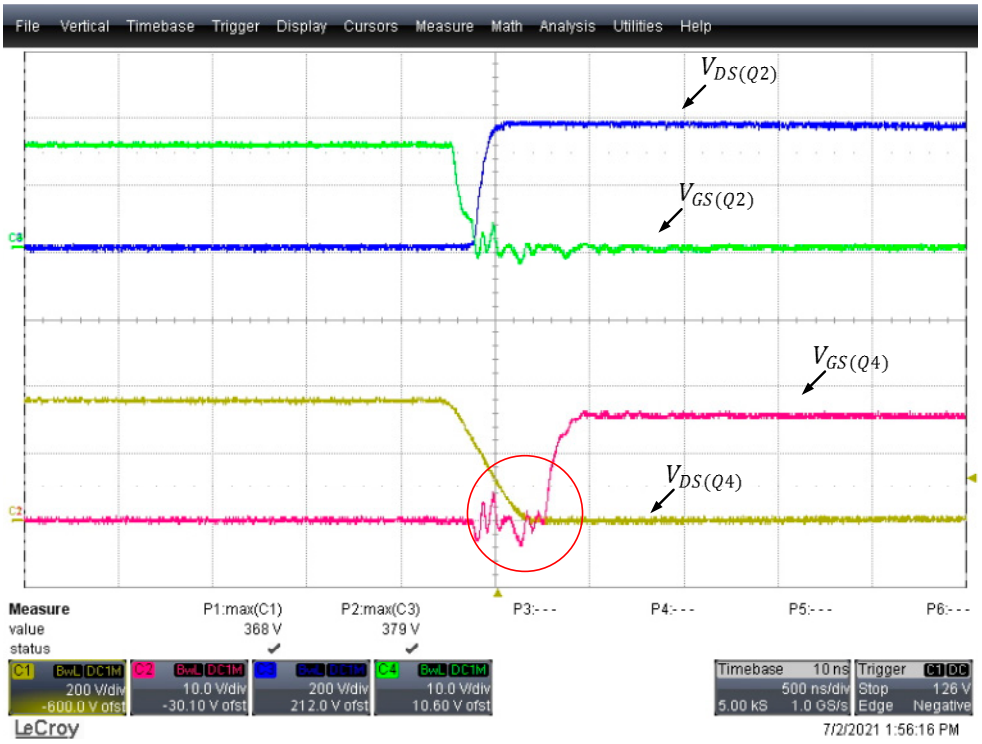

Figure 16. Parallel connection of the first-arm with excessive C_{oss}.

.

When the converter is under a heavy load, the copper loss and iron loss of the transformer is greater than the switching loss and conduction loss of the power transistors. Furthermore, adjusting the C_{oss} value does not significantly improve the efficiency. Hence, the C_{oss} experiment in this paper was conducted under a light load, where components with C_{oss} = 10 pF and 50 pF were connected parallel to each other; the observed efficiency changes are depicted in Figure 17. According to the empirical results, when the first-arm power transistors were connected in parallel to the component with C_{oss} = 70 pF, relative to a parallel connection with an unadjusted parasitic capacitance of 50 pF, the efficiency for 300 and 600 W were higher (92.603%vs.93.462% for 300 W) and (95.193% vs. 95.302% for 600 W).

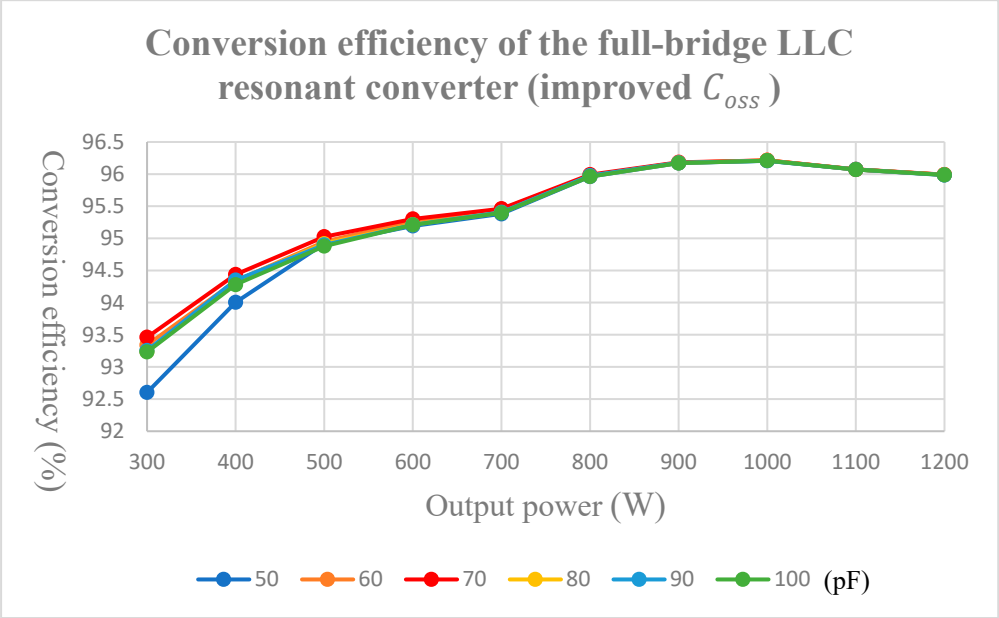

Figure 17. Conversion efficiency of the full-bridge LLC resonant converter (improved C_{oss}).

5. Conclusions

In this paper, a full-bridge LLC resonant converter was fabricated with a half-bridge LLC resonant controller chip that output higher power with the same input voltage, reducing the voltage stress on the power transistors and increasing the conversion efficiency. The first-arm power transistors were controlled with a controller chip, and the second-arm power transistors were driven with a coupling transformer loop. The converter dead time was extended by adjusting the C_{oss} of the first-arm power transistors to ensure that all four power transistors entered a ZVS state, thereby increasing the efficiency of the converter under a light load. Synchronous rectification was adopted on the secondary side to enhance the overall converter efficiency. Thus, a 1200 W full-bridge LLC resonant converter was achieved. In this experiment, when the output was 300 W, the converter efficiency increased from 92.603% to 93.462% and the maximum efficiency of the converter circuits reached 96.762%.

Author Contributions: Conceptualization, M.-H.C.; Methodology, M.-H.C.; Validation, M.-H.C. and C.-W.H.; Formal Analysis, M.-H.C.; Investigation, M.-H.C. and C.-W.H.; Writing-Original Draft Preparation, C.-W.H.; Writing-Review and Editing, M.-H.C.; Supervision, M.-H.C.; Project Administration, M.-H.C. All authors have read and agreed to the published version of the manuscript.

Funding: This article was subsidized by the Ming Chi University of Technology (MCUT), Taiwan (R.O.C.).

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Wang, P.; Cui, G.; Chen, L. Analysis and Design of LLC with new Current Driven Synchronous Rectifiers. In Proceedings of the 2011 International Conference on Electrical and Control Engineering, Yichang, China, 16–18 September 2011.
2. Ali, R.; Faraz, Z.A.; Noora, A.; Fareed, M.M.; Siyal, S.H. Computational Analysis of PT/CT Contact Behavior for a Heavy Water Reactor at High Temperature and Pressure. In Proceedings of the 2018 15th International Bhurban Conference on Applied Sciences and Technology (IBCAST), Islamabad, Pakistan, 9–13 January 2018.
3. Li, H.; Bai, L.; Zhang, Z.; Wang, S.; Tang, J.; Ren, X.; Li, J. A 6.6kW SiC bidirectional on-board charger. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018.
4. Zhang, F.; Yan, Y. Novel Forward–Flyback Hybrid Bidirectional DC–DC Converter. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1578–1584. [CrossRef]

5. Wei, X.; Zhao, X.; Dai, H. The application of flyback DC/DC converter in Li-ion batteries active balancing. In Proceedings of the 2009 IEEE Vehicle Power and Propulsion Conference, Dearborn, MI, USA, 7–10 September 2009.
6. Lim, C.Y.; Han, J.K.; Park, M.H.; Kim, K.W.; Moon, G.W. Phase-Shifted Full-Bridge DC-DC Converter With High Efficiency and Reduced Output Filter Using Center-Tapped Clamp Circuit. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2019.
7. Dutta, S.; Maiti, D.; Sil, A.K.; Biswas, S.K. A Soft-Switched Flyback Converter with Recovery of Stored Energy in Leakage Inductance. In Proceedings of the 2012 IEEE 5th India International Conference on Power Electronics (IICPE), Delhi, India, 6–8 February 2012.
8. Vu, H.N.; Tran, D.D.; Choi, W. A Novel Hybrid Soft Switching Full-Bridge PWM and Full-Bridge LLC Converter for On-Board Battery Charger Applications. In Proceedings of the 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, 22–26 May 2016.
9. Yan, J.; Zhao, X.; Chen, C.W.; Lai, J.S. Comparison of Secondary Topology of the LLC Converter for Photovoltaic Application. In Proceedings of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018.
10. Lan, G.; Zhang, S.; Wu, X. Analysis and Reduction of Common Mode Current of the Transformer in a Full-bridge LLC Battery Charger. In Proceedings of the 2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific), Harbin, China, 7–10 August 2017.
11. Peter, A.K.; Mathew, J. A Three-Level Half-Bridge Flying Capacitor Topology for Single-Stage AC-DC LLC Resonant Converter. In Proceedings of the 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 18–21 December 2018.
12. Chen, Q.; Wang, J.; Ji, Y.; Liang, S. Soft Starting Strategy of Bidirectional LLC Resonant DC-DC Transformer Based on Phase-Shift Control. In Proceedings of the 2014 9th IEEE Conference on Industrial Electronics and Applications, Hangzhou, China, 9–11 June 2014.
13. Ambatipudi, R.; Kotte, H.B.; Bertilsson, K. High Frequency (MHz) Planar Transformers for Next Generation Switch Mode Power Supplies. In Proceedings of the 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013.
14. Zhou, K.; Wang, X.; Yang, Q. Research on the performance of LLC resonant converter considering the influence of parasitic parameters. In Proceedings of the 2020 IEEE Sustainable Power and Energy Conference (iSPEC), Chengdu, China, 23–25 November 2020.
15. Liu, W.; Wang, B.; Yao, W.; Lu, Z.; Xu, X. Steady-State Analysis of the Phase Shift Modulated LLC Resonant Converter. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016.
16. Lin, B.R.; Du, Y.K. Analysis, Design and Implementation of a Wide ZVS Full-Bridge Converter. In Proceedings of the TENCON 2015–2015 IEEE Region 10 Conference, Macao, China, 1–4 November 2015.
17. Yazdani, M.R.; Farzanehfard, M. Evaluation and Comparison of Conducted EMI in Three Full-Bridge DC-DC Switching Converters. In Proceedings of the 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC), Shiraz, Iran, 12–14 February 2019.